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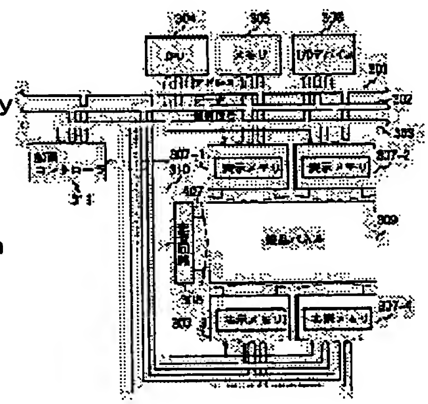
(54) DATA DRIVER AND LIQUID CRYSTAL DISPLAY DEVICE AND INFORMATION PROCESSING DEVICE USING IT.

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a liquid crystal display device which realizes a multi- gradation display and a moving video picture display which reducing the power consumption and the cost.

SOLUTION: Still-frame picture data are transferred from the CPU 304 to memory in a data driver 307 (307-1 to 307-4). Moving video picture data which require multi-gradation display are processed by a moving video picture driver 311 and sent to the data driver 307 through a panel 302. The regions of still- frame picture and moving picture in a liquid crystal panel 309 are preset in a register. In the still-frame picture display region, a selector selects the still- frame picture data sent from the memory. In the moving picture display region, the selector selects the moving picture data sent from the bus 302. The register, the latch, and the liquid crystal drive circuit impresses liquid crystal drive voltage on the data line of the liquid crystal panel 309 based on the data outputted by the selector.



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1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] In the data driver which outputs the liquid crystal driver voltage impressed to the data line of a liquid crystal panel according to the indicative data into which it is inputted from the outside The data bus into which an indicative data is inputted from the exterior, and the address bus into which the address is inputted from the exterior, It has an output bus for outputting the data read from the display memory and this display memory for memorizing an indicative data. It once stores in the field on the above-mentioned display memory which becomes settled based on the above-mentioned address into which the indicative data inputted through the above-mentioned data bus was inputted through the above-mentioned address bus. Then, the data-processing system which reads to the order which was able to define separately the indicative data stored in this display memory, and is outputted through the above-mentioned output bus, The data driver characterized by having a voltage-output means to output the liquid crystal driver voltage according to the data sent through the bus of the direction chosen by selection means to choose either the output bus of the above-mentioned data-processing system or the above-mentioned data buses, and the above-mentioned selection means.

[Claim 2] It is the data driver according to claim 1 carry out that the above-mentioned selection means is what is constituted including the selector which chooses either the above-mentioned data bus or the output bus of the above-mentioned data-processing system according to the directions from the memory which stores the selection information used as the criteria of selection, the directions circuit which outputs the selection directions according to the above-mentioned selection information, and the above-mentioned directions circuit as the description.

[Claim 3] It is the data driver according to claim 2 carry out that it is what issues the directions which choose the above-mentioned data bus, and takes out in the directions which choose the output bus of the above-mentioned data-processing system when other as the description during the period when the data which should be outputted to the field where the above-mentioned selection information specified the field on the above-mentioned liquid crystal panel at a field, and the above-mentioned directions circuit was specified by the above-mentioned selection information are sent through the above-mentioned data bus.

[Claim 4] The above-mentioned selection information is a data driver according to claim 3 characterized by specifying the field which displays the animation on the above-mentioned liquid crystal panel.

[Claim 5] the 1st gradation control circuit which performs gradation control based on the indicative data to which the above-mentioned data-processing system was read from the above-mentioned display memory — having — this — the data driver according to claim 1, 2, 3, or 4 characterized by being what outputs the data of Ushiro to whom gradation control by the 1st gradation control circuit was given through the above-mentioned output bus.

[Claim 6] The gradation control circuit of the above 1st is a data driver according to claim 5 characterized by being what performs the above-mentioned gradation control by the FRC method.

[Claim 7] the 2nd gradation control circuit which performs gradation control based on the above-mentioned data sent through the bus of the direction where the above-mentioned voltage-output means is chosen by the above-mentioned selection means — having — this — the data driver according to claim 1, 2, 3, 4, 5, or 6 characterized by to be what outputs the electrical potential difference obtained by gradation control by the 2nd gradation control circuit as the above-mentioned liquid crystal driver voltage.

[Claim 8] The gradation control circuit of the above 2nd is a data driver according to claim 7 characterized by

being what performs the above-mentioned gradation control by PWM or AM method.
[Claim 9] It is the liquid crystal display which is equipped with claims 1, 2, 3, 4, 5, 6, and 7 or a data driver given in eight, and the data controller that processes an indicative data, and is characterized by the above-mentioned data controller being what outputs data for the result of the above-mentioned processing to the above-mentioned data driver through the above-mentioned data bus.
[Claim 10] the 3rd gradation control circuit where the above-mentioned data controller performs gradation control to an indicative data — having — this — the liquid crystal display according to claim 9 characterized by being what outputs the data obtained by gradation control by the 3rd gradation control circuit.
[Claim 11] The gradation control circuit of the above 3rd is a liquid crystal display according to claim 10 characterized by being what performs the above-mentioned gradation control by the FRC method.
[Claim 12] the gradation control by the gradation control circuit of the above 1st, the gradation control by the gradation control circuit of the above 2nd, the gradation control by the gradation control circuit of the above 3rd, and ** — the liquid crystal display according to claim 10 characterized by performing a gradation display by combining at least two.
[Claim 13] The information processor characterized by having a liquid crystal display according to claim 10, 11, or 12.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the liquid crystal display and information processor which used a data driver and this.
[0002]
[Description of the Prior Art] The liquid crystal display is strongly expected low-power-ization not only for the purpose of improvement in display quality but for the purpose of loading to a pocket mold device. Therefore, display memory was built in the data driver LSI, and low-power-ization was attained by low-speed-izing the access frequency to the memory which stored the indicative data. Hereafter, such a conventional liquid crystal display is explained using drawing 18 , drawing 19 , and drawing 20 .
[0003] The principal part block diagram of a liquid crystal display and drawing 20 of the system configuration Fig. using the liquid crystal driver with built-in memory of the former [drawing 18] and drawing 19 are block diagrams with a detailed liquid crystal driver with built-in memory. What was shown here is a liquid crystal display which drives the liquid crystal panel 109 of 320x480 dots using four data drivers LSI 107 of 160 outputs.
[0004] In drawing 18 , the address bus attached sign"101." the same — " — 102 — " — a data bus — " — 103 — " — a control signal — a line — " — 104 — " — CPU — " — 105 — " — memory — " — 106 — " — an I/O device — " — 107 - one — " - " — 107 - four — " — display memory — having built — data — a driver - - LSI — " — 108 — " — a scanning circuit — " — 109 — " — a liquid crystal panel — " — 110 — " — a display — a synchronizing signal — ** — a signal line — pointing out — **** . In addition, the data driver LSI

107-1 to 107-4 may only be generically called the data driver LSI 107.

[0005] In drawing 19 and drawing 20 , the oscillator circuit for a display attached sign"201." It is the signal line which similarly transmits the control signal with which "202" shows the power circuit of a liquid crystal driver, and "203-1"-"203-4" shows the arrangement location of the data driver LSI 107-1 to 107-4. Hereafter, a control signal 203-1 to 203-4 may only be generically called a control signal 203. A line for a signal line for "204" to transmit a display-control signal and "205" to supply the supply voltage for scanning circuits and "206" have pointed out the line for supplying the supply voltage for data driver LSI107. The address administration circuit where "207" performs address control corresponding to a control signal 203, A signal line for "208" to transmit the column address obtained by address control by the address administration circuit 207, A signal line for "209" to transmit the row address of the display memory which performed address control in the address address administration circuit 207, The timing control circuit where "210" generates the various control signals of the data driver LSI107 interior based on a control signal 103, A signal line for "211" to transmit the control signal which controls I/O of an indicative data, A signal line for "212" to transmit the control signal which controls the row address 218 for a display, A signal line for "213" to transmit the control signal which controls a selector 221, A signal line for a signal line for "214" to transmit a latch signal and "215" to transmit the control signal which controls alternating current-ization of a liquid crystal drive, A signal line for the display address counter with which "217" generates the display address, and "218" to transmit the row address for a display, the I/O buffer to which "219" performs congruence directional control of data, and "220" have pointed out the data bus for transmitting data. As for the selector as which "221" chooses either the address for a display or the addresses which have been sent from the system (CPU104 grade), and "222", the selector 221 has pointed out the signal line for transmitting the row address chosen and outputted. The signal line for transmitting the selection signal with which the column address decoder generated "223" and the column address decoder 223 generated "224", and "225" point out the data selector of display memory 229, and "226" has pointed out the data bus of display memory 229. "227" has pointed out the row address decoder. The display memory to which "229" holds an indicative data (a memory cell, RAM), The signal line for transmitting the control signal with which "230" controls the display data bus from display memory 229, and "231" controls FRC data, A signal line for the FRC data circuit where "232" generates the data of FRC, and "233" to transmit FRC data, The FRC selector as which "234" chooses FRC data corresponding to an indicative data 230, A data bus for "235" to transmit the indicative data chosen by the FRC selector 234, The liquid crystal drive circuit which "236", the latch circuit to which "238" latches an indicative data, "237", and "239" are based on a display data bus, and "240" is based on an indicative data, and generates liquid crystal driver voltage, and "241" have pointed out the line for supplying liquid crystal driver voltage.

[0006] The sign which gave a signal, data, etc. to the signal line which transmits the signal concerned etc., and the bus may be attached and called into this specification. for example, the display synchronizing signal transmitted through a signal line 110 — "display synchronizing signal 110 — " — it may call Moreover, the indicative data transmitted through the display data bus 235 may be called "an indicative data 235."

[0007] Drive actuation of this liquid crystal display is explained using drawing 18 .

[0008] An indicative data is drawn by the display memory of the data driver LSI 107 from memory 105 or I/O device 106 according to control by CPU104. Drawing actuation of the indicative data to the data driver LSI 107 is performed by [as being the following] from this memory 105.

[0009] CPU104 performs the read cycle which once incorporates the data of memory 105 to the register of CPU104 with outputting the lead address and a control signal to memory 105. Then, CPU104 performs the light cycle which writes the data once incorporated to the register of CPU104 with outputting the light address and a control signal to the data driver LSI 107 in the display memory of the data driver LSI 107. CPU104 transmits the indicative data of memory 105 to the display memory of the data driver LSI 107 by repeating this actuation, and updates an indicative data (drawing).

[0010] Furthermore, detailed actuation of the data driver LSI 107 is explained using drawing 19 and drawing 20 .

[0011] The arrangement location to a liquid crystal panel 109 is set up by the control signal 203 with which each

data driver LSI 107 shows the arrangement location of a panel, respectively.

[0012] For this reason, as for four data drivers LSI 107, any have judged whether it is accessed to the address from CPU104 based on a control signal 203. If the light address from CPU104 is received, the address administration circuit 207 will judge whether the address concerned is the address which the data driver LSI 107 to which oneself belongs takes charge of. When it is the address which the data driver LSI 107 to which oneself belongs takes charge of as a result of a judgment, the address concerned is changed into the address (a column address 208, row address 209) of display memory 229, and this is outputted to the column address decoder 223 and a selector 221.

[0013] At the time of the light cycle from CPU104, a selector 221 chooses a row address 209 and outputs this to the row address decoder 227. Then, the row address decoder 227 chooses the gate line of the display memory 229 corresponding to the address. On the other hand, the column address decoder 223 is confirming the data selector 225 corresponding to a column address 208, and chooses the data line of display memory 229. Thereby, the light data 220 from I/O buffer 219 can be written in the predetermined address of display memory 229. An indicative data is updated by repeating the above actuation (drawing).

[0014] The x2 bit (4 gradation) indicative data is held by one screen at display memory 229.

[0015] In the case of read-out of the indicative data from display memory 229, a selector 221 chooses the row address (display address) 218 generated with the display address counter 217. Thereby, the indicative data of every one line of the address specified by the display address 218 at that time is read one by one by the FRC selector 234. This read-out is performed synchronizing with a Horizontal Synchronizing signal. The FRC selector 234 outputs the read indicative data to a latch circuit 236 as a 1-bit indicative data 235. A sequential transfer is carried out by the latch circuit 236,238 as an indicative data 237,239, and this indicative data 235 is inputted into the liquid crystal drive circuit 240. The liquid crystal drive circuit 240 generates the liquid crystal driver voltage 241 corresponding to this indicative data 239, and drives a liquid crystal panel 109.

[0016] A scanning circuit 108 confirms the gate line of one line of a liquid crystal panel 109 at a time one by one synchronizing with this. A display will be performed by this.

[0017] In addition, a latch circuit is constituted in two steps (a latch circuit 236, latch circuit 238), and mediation actuation when access (writing to display memory 229) and the display action (read-out from display memory 229) from CPU104 compete is performed by controlling each timing of operation by the latch signal 214,215 here.

[0018]

[Problem(s) to be Solved by the Invention] By the way, the display of an animation is increasingly required with development of a multimedia technique in recent years. In order to display an animation, the multi-gradation display of 32 or more gradation will be indispensable practically. In order to display 1-pixel 32 gradation, 1-pixel a 5-bit indicative data is needed. And in order to realize this with the above-mentioned conventional technique, the capacity of the memory built in the data driver LSI must be made to increase.

[0019] However, if the capacity of the memory to build in is made to increase, a chip size will increase, and it becomes difficult to attain low-pricing. Moreover, although renewal of 30 or more frames is required for the drawing data of an animation in 1 second, for that purpose, data must be transmitted for every frame, and high-speed rewriting of memory becomes indispensable. If the number of gradation increases, in order for the amount of data to also increase, therefore the number of gradation increases, as for rewriting, improvement in the speed comes to be required further. Such improvement in the speed leads to increase of power consumption. Thus, it was difficult to realize low-power-izing and low cost-ization to ** with the conventional technique.

[0020] This invention aims at offering the liquid crystal display using the data driver and this which can respond to a movie display, and an information processor, realizing low cost and a low power.

[0021]

[Means for Solving the Problem] In this invention, an animation controller is formed apart from a data driver, and it is made to perform processing for animation processing and a liquid crystal multi-gradation display here. The data processed through the display memory in a data driver are used for the display of a still picture. On the other hand, the data sent from an animation controller are used for the display of an animation. By using it

according to a viewing area, changing both, it can respond to an animation, without causing increase of power consumption, and increase of the capacity of display memory. That is, in the still picture from which the display screen does not change,-izing of the access frequency of display memory can be carried out [low speed] (if every one line is read from display memory, access to display memory is sufficient for a level period at once). On the other hand, it is not necessary to make the display memory capacity built in a data driver increase by making it process for an animation controller by the movie display. Moreover, in order to process gradation control by the animation controller, the number of gradation displays is not restricted by only the data driver. If the gradation control by the data driver and the gradation control by the animation controller are combined, the number of gradation displays can be made [more].

[0022] It will be as follows if the configuration of this invention is described more concretely.

[0023] In the data driver which outputs the liquid crystal driver voltage impressed to the data line of a liquid crystal panel as the 1st mode of this invention according to the indicative data into which it is inputted from the outside The data bus into which an indicative data is inputted from the exterior, and the address bus into which the address is inputted from the exterior, It has an output bus for outputting the data read from the display memory and this display memory for memorizing an indicative data. It once stores in the field on the above-mentioned display memory which becomes settled based on the above-mentioned address into which the indicative data inputted through the above-mentioned data bus was inputted through the above-mentioned address bus. Then, the data-processing system which reads to the order which was able to define separately the indicative data stored in this display memory, and is outputted through the above-mentioned output bus, A selection means to choose either the output bus of the above-mentioned data-processing system or the above-mentioned data buses, The data driver characterized by having a voltage-output means to output the liquid crystal driver voltage according to the data sent through the bus of the direction chosen by the above-mentioned selection means is offered.

[0024] It is [means / above-mentioned / selection] desirable in it being what is constituted including the selector which chooses either the above-mentioned data bus or the output bus of the above-mentioned data-processing system according to the directions from the memory which stores the selection information used as the criteria of selection, the directions circuit which outputs the selection directions according to the above-mentioned selection information, and the above-mentioned directions circuit.

[0025] It is desirable in it being what the directions which choose the above-mentioned data bus issue during the period when the data which should be outputted to the field where the above-mentioned selection information specified the field on the above-mentioned liquid crystal panel, and the above-mentioned directions circuit was specified by the above-mentioned selection information are sent through the above-mentioned data bus, and takes out in the directions which choose the output bus of the above-mentioned data-processing system when other.

[0026] The above-mentioned selection information may specify the field which displays the animation on the above-mentioned liquid crystal panel.

[0027] the 1st gradation control circuit which performs gradation control based on the indicative data to which the above-mentioned data-processing system was read from the above-mentioned display memory — having — this — data after gradation control by the 1st gradation control circuit was performed may be outputted through the above-mentioned output bus.

[0028] The gradation control circuit of the above 1st may perform the above-mentioned gradation control by the FRC method.

[0029] the 2nd gradation control circuit which performs gradation control based on the above-mentioned data sent through the bus of the direction where the above-mentioned voltage-output means is chosen by the above-mentioned selection means — having — this — the electrical potential difference obtained by gradation control by the 2nd gradation control circuit may be outputted as the above-mentioned liquid crystal driver voltage.

[0030] The gradation control circuit of the above 2nd may perform the above-mentioned gradation control by PWM or AM method.

[0031] As the 2nd mode of this invention, it has the data driver of the 1st mode mentioned above, and the data controller which processes an indicative data, and the liquid crystal display characterized by the above-mentioned data controller being what outputs data for the result of the above-mentioned processing to the above-mentioned data driver through the above-mentioned data bus is offered.
[0032] the 3rd gradation control circuit where the above-mentioned data controller performs gradation control to an indicative data — having — this — it is desirable that it is what outputs the data obtained by gradation control by the 3rd gradation control circuit.
[0033] The gradation control circuit of the above 3rd may perform the above-mentioned gradation control by the FRC method.
[0034] the gradation control by the gradation control circuit of the above 1st, the gradation control by the gradation control circuit of the above 2nd, the gradation control by the gradation control circuit of the above 3rd, and ** — a gradation display may be performed by combining at least two.
[0035] The information processor characterized by having the liquid crystal display of the 2nd above-mentioned mode as the 3rd mode of this invention is offered.
[0036] The operation of each mode mentioned above is explained collectively.
[0037] By the data-processing system, the indicative data inputted through the data bus is once stored in display memory. The storing field at this time is appointed based on the address inputted through the address bus. Then, it reads to the order which was able to define separately the indicative data stored in display memory, and outputs through an output bus. In addition, when the data-processing system has the 1st gradation control circuit, data after gradation control (for example, gradation control by the FRC method) by this 1st gradation control circuit was performed to the indicative data read from display memory are outputted to an output bus.
[0038] A data controller outputs data for the result of having processed the indicative data to a data driver through a data bus. In addition, when the data controller has the 3rd gradation control circuit, the data obtained by gradation control (for example, gradation control by the FRC method) by this 3rd gradation control circuit are outputted.
[0039] A selection means chooses either the output bus of a data-processing system or the data buses. According to the selection directions according to selection information which a directions circuit outputs, this selection means is realizable because a selector chooses either a data bus or the output bus of a data-processing system. When this selection information specifies the field on a liquid crystal panel (for example, animation display field), a directions circuit issues the directions which choose a data bus during the period when the data which should be outputted to the field specified by this selection information are sent from a data controller through a data bus. When other, the directions which choose the output bus of a data-processing system are issued.
[0040] A voltage-output means outputs the liquid crystal driver voltage according to the data sent through the bus of the direction chosen by the selection means. In addition, when the voltage-output means has the 2nd gradation control circuit, the electrical potential difference obtained by performing gradation control (for example, gradation control by PWM or AM method) by this 2nd gradation control circuit to the inputted data is outputted as liquid crystal driver voltage.
[0041]
[Embodiment of the Invention] The operation gestalt of this invention is explained using a drawing.
[0042] The liquid crystal display which is the 1st operation gestalt of this invention is explained using drawing 1 thru/or drawing 5 , drawing 10 , or drawing 15 .
[0043] First, an outline is explained using drawing 1 .
[0044] This liquid crystal display consists of the 320x480-pixel liquid crystal panel 309, the data driver LSI 307-1 to 307-4 and a scanning circuit 308, the animation controller 311, CPU304, memory 305, and I/O device 306. And it connects between these each part by the address bus 301, the data bus 302, the control signal line 303, and the display synchronizing signal line 310. In addition, in explanation after this, the data driver LSI 307-1 to 307-4 may only be generically called "the data driver LSI 307." Moreover, the sign of a signal line which transmits the

signal concerned for a signal among this specification may be attached and called. For example, the display synchronizing signal sent through the display synchronizing signal line 310 may be called "the display synchronizing signal 310."

[0045] CPU304 has come to be able to carry out direct access to the display memory which the data driver LSI 307 builds in through an address bus 301 and a data bus 302. Moreover, the animation controller 311 can access the data driver LSI 307 now through an address bus 301 and a data bus 302 similarly. This updates an indicative data by CPU304 and memory 305 about still picture data in this liquid crystal display (drawing). On the other hand, about a video data, it is outputted to the data driver LSI 307 from the animation controller 311. And the data driver LSI 307 equips the interior with the information which shows an animation display field, changes the indicative data (still picture data) sent from CPU304 grade, and the indicative data (video data) sent from the animation controller 311 according to this information, and outputs it to a liquid crystal panel 309.

[0046] The description on the configuration for realizing such actuation is mainly in the data driver LSI 307. Then, suppose after this that it explains focusing on the data driver LSI 307.

[0047] Each data driver LSI 307 is equipped with the display memory (memory cell 433) equipped with the capacity which can hold the indicative data of 2 bits of each pixel by 240 lines only 160 ****. Therefore, a 160x240-pixel liquid crystal panel can be displayed with 4 gradation by one data driver LSI 307. Since a liquid crystal panel 309 is 320x480 pixels, it arranges every (a total of four pieces) two of this data driver LSI 307 up and down, and performs 2 screen drives of the upper and lower sides of every 240 lines.

[0048] The data driver LSI 307 is equipped with the address administration circuit 408, the timing control circuit 411, I/O buffer 419, the display address counter 421, a selector 423, the row address decoder 425, the FRC data circuit 427, the column address decoder 429, a data selector 431, a memory cell 433, the FRC selector 435, the selector 437, the shift register 439, the latch circuit 441, and the liquid crystal drive circuit 443 as shown in drawing 2 and drawing 3 . Moreover, it has the various signal lines for connecting between these each part (or between other circuit parts), and bus 420,432,434,442 grade.

[0049] In addition, the oscillator circuit 402 and power circuit 404 which were not being omitted and drawn in drawing 1 are also drawn on this drawing 2 and drawing 3 .

[0050] The address administration circuit 408 changes the address 301 into a column address 409 and a row address 410 based on a control signal 303,401. On the other hand, the address administration circuit 408 is outputting the row address 410 for the column address 409 to the column address decoder 429 through a selector 423 to the row address decoder 425. In addition, a control signal 401 is for specifying any are the candidates for access at that time among four data drivers LSI 307.

[0051] The timing control circuit 411 generates the various control signals 412, 413, 414, 415, and 416,417,418,445 of the data driver LSI307 interior from a control signal 303 and the display synchronizing signal 310. The control signal 412 is outputted to I/O buffer 419 among these control signals. The control signal 413 is outputted to the display address counter 421. The control signal 414 is outputted to the selector 423. The control signal 415 is outputted to the FRC data circuit 427. The shift clock 416 is outputted to the shift register 439. The latch signal 417 is outputted to the latch circuit 441, and is used for controlling the timing which latches an indicative data. The control signal 418 is outputted to the liquid crystal drive circuit 443, and is used for controlling alternating current-ization of a liquid crystal drive. The control signal 445 is outputted to the selector 437, and is used for choosing either between two data buses (a data bus 436, data bus 302) connected to the selector 437. In addition, the above-mentioned control signal 401 is inputted also into the timing control circuit 411.

[0052] This timing control circuit 411 is equipped with the register 4110 with which the information which shows the field where an animation is displayed on a liquid crystal panel 309 was stored. Moreover, the row address 422 which shows whether the indicative data corresponding to Rhine of what position on a liquid crystal panel 309 should be read from a memory cell 433 is then inputted into this timing control circuit 411. The control signal 445 is generated based on the contents and the row address 422 of this register 4110. That is, in the animation display field, the control signal 445 is generated so that an indicative data 436 (still picture data) may be made to

choose as a selector 437 an indicative data 302 (video data sent from the animation controller 311) by the still picture viewing area on the other hand. Such a point is the focus of this operation gestalt max.

[0053] I/O buffer 419 controls I/O of an indicative data 302,420 according to a control signal 412.

[0054] The display address counter 421 generates the row address 422 for a display according to a control signal 413. This display address counter 421 is outputting this row address 422 to the timing control circuit 411 and the selector 423.

[0055] A selector 423 chooses either the row address 422 for a display or the row addresses 410 for drawing according to a control signal 414. This selector 423 is outputting the selected one to the row address decoder 425 as a row address 424.

[0056] The row address decoder 425 generates the WORD selection signal 426 by decoding a row address 424, and outputs this to the gate line of a memory cell 433.

[0057] The column address decoder 429 generates a selection signal 430 based on a column address 409. This column address decoder 429 is outputting this selection signal 430 to the data selector 431.

[0058] A data selector 431 is choosing the data line of the data bus 432 of a memory cell 433 according to a selection signal 430, and controls I/O of the indicative data 420 to a memory cell 433.

[0059] A memory cell 433 is the memory for storing temporarily an indicative data (still picture data), and consists of RAM. The field set as the object of writing/read-out of the indicative data on this memory cell 433 can be specified now based on an above-mentioned column address and an above-mentioned row address. The memory cell 433 of this operation gestalt is equipped with the capacity which can hold the indicative data of 2 bits of each pixel by 240 lines only 160 **** as mentioned above.

[0060] The FRC data circuit 427 and the FRC selector 435 are for performing the gradation display by the FRC method. It is changing applied voltage (namely, display brightness) for every frame, and is the method which displays the brightness of middle gradation as it is indicated in drawing 15 as an FRC gradation method (in the example of drawing 15 , display brightness is changed by the odd frame and even frames). In case the FRC data circuit 427 performs a gradation display with an FRC gradation method, it generates the required FRC data 428. The generation timing of the FRC data 428 is determined according to the control signal 415. The FRC selector 435 performs processing (FRC control) which chooses 1 bit of FRC data corresponding to the 1-pixel 2-bit indicative data 434. The FRC selector 435 is outputting the data generated by FRC control to the selector 437 as an indicative data 436.

[0061] the indicative data 302 (video data) into which the selector 437 is inputted as the indicative data 436 (still picture data) from the animation controller 311, and ** — inner either is chosen according to a control signal 445. That is, in this operation gestalt, by the time the indicative data sent through a data bus 302 results in a selector 437, the two roots will be prepared. The 1st root is after data bus 302 the root which results in a selector 437 through I/O buffer 419, a data selector 431, a memory cell 433, the FRC selector 435, and a data bus 436. The 2nd root is the root which connected the data bus 302 to the selector 437 directly through the memory cell 433 grade. During the period which should input the indicative data about the field beforehand set up as an animation display field, the video data is inputted into the data bus 302 from the animation controller 311. Still picture data are inputted into the data bus 302 from CPU304 and the memory 305 grade during the period which should, on the other hand, input the indicative data about the field beforehand set up as a quiescence viewing area. Therefore, in a selector 437, either of the two roots from a data bus 302 to a selector 437 can be chosen now according to an indicative data by choosing either of a data bus 436 and a data bus 302 according to a control signal 445. This selector 437 is outputted to the shift register 439 by making into an indicative data 438 the direction which carried out in this way and was chosen.

[0062] In addition, the concrete internal configuration of the selector 437 in this operation gestalt was shown in drawing 4 .

[0063] A shift register 439 is a 8-bit bidirectional shift register, and is operating according to the shift clock (control signal) 416.

[0064] A latch circuit 441 latches an indicative data (getting it blocked and synchronizing with the display

selection signal 407 of a scanning circuit 308) 440 according to a control signal 417. This latch circuit 441 is outputting the latched data to the liquid crystal drive circuit 443 as an indicative data 442.
[0065] The liquid crystal drive circuit 443 generates the liquid crystal driver voltage 444 corresponding to an indicative data 442.
[0066] An oscillator circuit 402 generates the display clock 403 for specifying display timing, and supplies it to a scanning circuit 308.
[0067] A power circuit 404 generates and supplies liquid crystal panel driver voltage (the supply voltage 405 for scanning circuit 308, supply voltage 406 for data driver LSI307).
[0068] Next, the display action in this operation gestalt is explained.
[0069] Explanation is divided into the display action of a still picture, and the display action of an animation, and is performed.
[0070] what CPU304 reads and (read access) carries out the indicative data in memory 305 about a [display action of still picture] still picture, and this is written in the memory cell 433 of the data driver LSI 307 for (light access) — it is — the renewal of an indicative data (drawing) — it is carried out. Access to memory 433 is performed at random. Access of CPU304 at this time is performed by the SRAM interface. The read/write timing of a SRAM interface was shown in drawing 10 and drawing 11 . The address signal is transmitted through the address bus 301 among the signals shown in drawing 10 and drawing 11 . The data signal is transmitted through the data bus 302. Signals other than this are included in the control signal 303.
[0071] Hereafter, the writing of the indicative data to the memory cell 433 of the data driver LSI 307 and read-out of the indicative data from a memory cell 433 are explained.
[0072] First, the writing of the indicative data to a memory cell 433 is explained.
[0073] The read/write address from a system (CPU304 grade) is inputted into the address administration circuit 408 of the data driver LSI 307 through an address bus 301. As for the address administration circuit 408 of each data driver LSI 307, based on a control signal 401, access at that time judges whether it is a thing to its data driver LSI 307 which belongs, respectively. When it is access to the data driver LSI 307 to which oneself belongs as a result of this judgment, the address 301 inputted at this time is changed into a column address 409 and a row address 410.
[0074] The column address decoder 429 decodes this column address 409. A data selector 431 chooses the data line of the corresponding address based on this decoding result.
[0075] On the other hand, a selector 423 chooses a row address 410 and outputs it to the row address decoder 425 as a row address 424. The row address decoder 425 decodes this row address 424, and chooses one gate line according to a decoding result. Thereby, CPU304 can access the predetermined bit on the memory cell 433 which becomes settled by the data line and the gate line which are then chosen, and can transmit an indicative data to the predetermined address.
[0076] Next, read-out (display action) of the indicative data from a memory cell 433 is explained.
[0077] The FRC selector 435 changes into the 1-bit FRC data 436 the indicative data (data of 2 bits of each pixel for one line) held at the memory cell 433.
[0078] By the way, the timing control circuit 411 is checking the contents and the row address 422 of a register 4110, and knows displaying the still picture field at this time. Therefore, the timing control circuit 411 is outputting a value as which a selector 437 chooses a data bus 436 as a control signal 445 at this time. According to this control signal 445, a selector 437 chooses a data bus 436 and outputs the FRC data sent through this data bus 436 as an indicative data 438.
[0079] A shift register 439 latches an indicative data 438 a level period. The latch circuit 441 following this is the following level period, latches the indicative data 440 which a shift register 439 outputs, and outputs it to the liquid crystal drive circuit 443 as an indicative data 442. The liquid crystal drive circuit 443 chooses the liquid crystal driver voltage 444 corresponding to this indicative data 442, and outputs it to a liquid crystal panel 309. The output of the liquid crystal driver voltage 444 is outputted synchronizing with the scan selection electrical potential difference 407 which a scanning circuit 308 generates, and, thereby, can realize the display for one line

of a iiquid crystal panel 309.

[0080] The display of a still picture is attained by repeating the above actuation.

[0081] In displaying a [display action of animation] animation, a multi-gradation display and the fast transfer of an indicative data are needed in practice. Since the data driver LSI 307 of this operation gestalt corresponds to this, it performs the following drawing actuation.

[0082] A video data performs animation expanding processing from animation compressed data by the animation controller 311 and CPU304, and develops it to an indicative data. As for the developed indicative data, the animation controller 311 performs FRC control.

[0083] By the way, the animation controller 311 is also equipped with the register (control register circuit 505 in drawing 5 mentioned later) which stored the information which shows an animation field. The animation controller 311 can know whether the animation display field is then set as the object of display processing by checking the contents of this register etc. When the animation display field is then set as the object of display processing, the animation controller 311 performs above-mentioned FRC control. And the 1-bit FRC data of every one line obtained as a result are sent to the data driver LSI 307 through a data bus 302 one by one.

[0084] It gets to know that it is an animation display field that the timing control circuit 411 of the data driver LSI 307 is also then set as the object of display processing by checking the contents and the row address 422 of a register 4110 similarly. Therefore, let the timing control circuit 411 be the value as which a selector 437 chooses a data bus 302 for the control signal 445 at this time. Consequently, a selector 437 chooses the FRC data sent from the animation controller 311 through a data bus 302, and is made to output them to a shift register 439. The output of the liquid crystal driver voltage 444 based on this FRC data will be performed like the case of a still picture after this.

[0085] Next, the timing of the animation data transfer to the data driver LSI 307 and the timing of processing within the data driver LSI 307 of this video data are further explained to a detail using drawing 12 , drawing 13 , and drawing 14 from the animation controller 311.

[0086] In explanation here, the field (n<m) from n lines of a liquid crystal panel 309 to m lines shall be set up as an animation display field in the register 4110 of the timing control circuit 411 (refer to drawing 12).

[0087] Animation display data of every one line are transmitted to the data driver LSI 307 from the animation controller 311 through a data bus 302 at a serial. In drawing 13 , CL1 is a synchronizing signal showing a level period, and is a signal included in the display synchronizing signal 310 (refer to drawing 2 and drawing 3).

[0088] The timing control circuit 411 is outputted to the display address counter 421 by making this CL1 into a control signal 413. The display address counter 421 counts this control signal 413 (CL1), and is outputting that counted value to the selector 423 as a row address 422 for a display.

[0089] Although the selector 437 has changed the selection condition according to the control signal 445, the selection condition has the counted value and the following relation of the display address counter 421. That is, when the counted value of the display address counter 421 is n−1, the selector 437 has chosen the data bus 436 (that is, FRC data obtained based on the indicative data of the n−1st line stored in the memory cell 433) (when it is not an animation display field). When the counted value of the display address counter 421 is n, the selector 437 has chosen the data bus 302 (that is, indicative data sent from the animation controller 311) (when it is an animation display field). Thus, in an animation display field, a selector 437 chooses a data bus 302 (indicative data from the animation controller 311), and the indicative data of a memory cell 433 is chosen except an animation display field.

[0090] Moreover, actuation of the animation controller 311 also has actuation and the following relation of a selector 437 and the display address counter 421. That is, when the display counter 421 counts (n−1), the animation controller 311 carries out the sequential transfer of the indicative data of the n−th line.

[0091] In the data driver LSI 307, the data (one line) of the n−th line with which the shift register 439 has been sent from this animation controller 311 to the timing shown in drawing 14 are incorporated. That is, a shift register 439 is the shift clock 416 which synchronized with WE signal, and incorporates an indicative data 438 (the data of the n−th line sent from the animation controller 311) by one line one by one (notes: at this time, the selector 437

is made into the condition of having chosen the data bus 302 as already stated). In addition, the transfer of the indicative data from the animation controller 311 is performed synchronizing with WE signal (write enable signal) in drawing 14 . A shift register 439 transmits the data incorporated to such timing to a latch circuit 441 as an indicative data 440.

[0092] A latch circuit 441 latches this indicative data 440 synchronizing with the CL1 following signal, and transmits it to the liquid crystal drive circuit 443 as an indicative data 442 (refer to drawing 13). The liquid crystal drive circuit 443 generates and outputs the liquid crystal driver voltage 444 according to this indicative data 442. The output of the liquid crystal driver voltage 444 is outputted synchronizing with the scan selection electrical potential difference 407 which a scanning circuit 308 generates, and, thereby, can realize the display for one line of a liquid crystal panel 309.

[0093] A movie display becomes possible by repeating the above actuation.

[0094] The animation controller 311 is explained using drawing 5 .

[0095] The animation controller 311 elongates compressed data, such as MPEG, and reproduces an indicative data. This animation controller 311 is equipped with the timing control circuit 501, the I/O-hardware-control circuit 502 which controls I/O, the address control circuit 503, the animation processing circuit 504, the control register circuit 505, and the FRC control circuit 506 as it is shown in drawing 5 . Moreover, it has the signal lines 507, 508, and 509,510,511,512 and address bus 513,514 which connect these each part, and data buses 515, 516, and 517,518,519,520.

[0096] The I/O-hardware-control circuit 502 is controlling I/O of the data signal which leads a data bus 302, and I/O of the address signal which leads an address bus 301. The I/O-hardware-control circuit 502 outputs the compressed data inputted through the data bus 302 to the animation processing circuit 504. Moreover, the address signal inputted through the address bus 301 is outputted to the address control circuit 503.

[0097] The animation processing circuit 504 processes expanding of the inputted compressed data, playback, the scaling that was adapted for the display size. And the indicative data obtained by this processing is outputted to the FRC control circuit 506. The FRC control circuit 506 changes this indicative data into FRC data. This FRC data is again returned to the I/O-hardware-control circuit 502 through the animation processing circuit 504 after this.

[0098] The information which shows the animation display field then set up is stored in the control register circuit 505. The I/O-hardware-control circuit 502 is checking the contents of this control register circuit 505, and it gets to know whether display processing to an animation field is then performed. And only when the display process to an animation field is performed, FRC data are outputted through a data bus 302. It is as relation with the timing of the data driver LSI 307 of operation having been shown in above-mentioned drawing 13 and drawing 14 .

[0099] The timing of each part in the animation controller 311 of operation is adjusted based on the various control signals 507 and 508,509,510,511 in which the timing control circuit 501 carries out a generation output based on a control signal 303. Moreover, management of the address is made by the address control circuit 503.

[0100] In the liquid crystal display of this operation gestalt, the memory cell 433 with which the data driver LSI 307 is equipped is used only for the still picture display as explained above. Therefore, it is not necessary to rewrite a memory cell 433 at a high speed, and low-power-izing is possible. Moreover, the animation controller is performing FRC control for the gradation display in a movie display. Therefore, animation display (this operation gestalt 32 gradation) of many gradation becomes realizable easily, without increasing the memory space of the data driver LSI 307.

[0101] The liquid crystal display which is the 2nd operation gestalt of this invention is explained using drawing 6 , drawing 7 , drawing 10 or drawing 14 , and drawing 16 .

[0102] With the 2nd operation gestalt, pulse width modulation (PWM) is used as a gradation method.

[0103] This whole liquid crystal display configuration is the same as that of the 1st operation gestalt (refer to drawing 1) except for the point of using the data driver 900 instead of the data driver 307. this — the description in the 2nd operation gestalt is mainly in the data driver LSI 900. Then, suppose after this that it explains focusing on the data driver LSI 900.

[0104] Each data driver LSI 900 is equipped with the display memory (memory cell 933) equipped with the capacity which can hold the indicative data of 2 bits of each pixel by 240 lines only 160 ****. Therefore, a 160x240-pixel liquid crystal panel can be displayed with 4 gradation by one data driver LSI 900. Since a liquid crystal panel 309 is 320x480 pixels, it arranges every (a total of four pieces) two of this data driver LSI 900 up and down, and performs 2 screen drives of the upper and lower sides of every 240 lines.
[0105] The data driver LSI 900 is equipped with the address administration circuit 908, the timing control circuit 911, I/O buffer 919, the display address counter 921, a selector 923, the row address decoder 925, the column address decoder 929, a data selector 931, a memory cell 933, the selector 937, the shift register 939, the latch circuit 941, and the liquid crystal drive circuit 943 as shown in drawing 6 and drawing 7 . Moreover, it has the various signal lines for connecting between these each part (or between other circuit parts), and bus 920,932,934,942 grade.
[0106] In addition, the oscillator circuit 402 and power circuit 904 which were not being omitted and drawn in drawing 1 are also drawn on this drawing 6 and drawing 7 .
[0107] The address administration circuit 908 changes the address 301 into a column address 909 and a row address 910 based on a control signal 303,901. On the other hand, the address administration circuit 908 is outputting the row address 910 for the column address 909 to the column address decoder 929 through a selector 923 to the row address decoder 925. In addition, a control signal 901 is for specifying any are the candidates for access at that time among four data drivers LSI 900.
[0108] The timing control circuit 911 generates the various control signals 912, 913, 914, 916, and 917,918,927,945 of the data driver LSI900 interior from a control signal 303 and the display synchronizing signal 907. The control signal 912 is outputted to I/O buffer 919 among these control signals. The control signal 913 is outputted to the display address counter 921. The control signal 914 is outputted to the selector 923. The control signal (shift clock) 916 is outputted to the shift register 939. The control signal (latch signal) 917 is outputted to the latch circuit 941, and is used for controlling the timing which latches an indicative data. The control signal 918 is outputted to the liquid crystal drive circuit 943, and is used for controlling alternating current-ization of a liquid crystal drive. The control signal 927 is outputted to the liquid crystal drive circuit 943, and is used for controlling the timing of Pulse Density Modulation. The control signal 945 is outputted to the selector 937, and is used for this selector 937 choosing either between two data buses (a data bus 436, data bus 302) connected to the selector 937. In addition, the above-mentioned control signal 901 is inputted also into the timing control circuit 911.
[0109] This timing control circuit 911 is equipped with the register 9110 with which the information which shows the field where an animation is displayed on a liquid crystal panel 309 was stored. Moreover, the row address 922 which shows whether the indicative data corresponding to Rhine of what position on a liquid crystal panel 309 should be read from a memory cell 933 is then inputted into this timing control circuit 911. The above-mentioned control signal 945 is generated based on the contents and the row address 922 of this register 9110. That is, in the animation display field, the control signal 945 is generated so that an indicative data 934 (still picture data) may be made to choose as a selector 937 an indicative data 302 (video data sent from the animation controller 311) by the still picture viewing area on the other hand. Such a point is the focus of this operation gestalt max.
[0110] I/O buffer 919 controls I/O of an indicative data 302,920 according to a control signal 912.
[0111] The display address counter 921 generates the row address 922 for a display according to a control signal 913. This display address counter 921 is outputting this row address 922 to the timing control circuit 911 and the selector 923.
[0112] A selector 923 chooses either the row address 922 for a display or the row addresses 910 for drawing according to a control signal 914. This selector 923 is outputting the selected one to the row address decoder 925 as a row address 924.
[0113] The row address decoder 925 generates the WORD selection signal 926 by decoding a row address 924, and outputs this to the gate line of a memory cell 933.
[0114] The column address decoder 929 generates a selection signal 930 based on the column address 909 which

the address administration circuit 908 outputs. This column address decoder 929 is outputting this selection signal 930 to the data selector 931.

[0115] A data selector 931 is choosing the data line of the data bus 933 of a memory cell 933 according to a selection signal 930, and controls I/O of the indicative data 920 to a memory cell 933.

[0116] A memory cell 933 is the memory for storing temporarily an indicative data (still picture data), and consists of RAM. The field set as the object of writing/read-out of the indicative data on this memory cell 933 can be specified now based on an above-mentioned column address and an above-mentioned row address. The memory cell 933 is equipped with the capacity which can hold the indicative data of 2 bits of each pixel by 240 lines only 160 **** as mentioned above.

[0117] the indicative data 302 (video data) into which the selector 937 is inputted as the indicative data 934 (still picture data) from the animation controller 311, and ** — inner either is chosen according to a control signal 945. That is, in this operation gestalt, by the time the indicative data sent through a data bus 302 results in a selector 937, the two roots will be prepared. The 1st root is after data bus 302 the root which results in a selector 937 through I/O buffer 919, a data selector 931, a memory cell 933, and a data bus 934. The 2nd root is the root which connected the data bus 302 to the selector 937 directly through the memory cell 933 grade. During the period which should input the indicative data about the field beforehand set up as an animation display field, the video data is inputted into the data bus 302 from the animation controller 311. Still picture data are inputted into the data bus 302 from CPU304 and the memory 305 grade during the period which should, on the other hand, input the indicative data about the field beforehand set up as a quiescence viewing area. Therefore, in a selector 937, either of the two roots from a data bus 302 to a selector 937 can be chosen now according to an indicative data by choosing either a data bus 934 or the data buses 302 according to a control signal 945. This selector 937 is outputted to the shift register 939 by making into an indicative data 938 the direction which carried out in this way and was chosen.

[0118] In addition, the concrete internal configuration of the selector 937 in this operation gestalt is [the selector 437 in the 1st operation gestalt, and] the same (refer to drawing 4).

[0119] A shift register 939 is a 8-bit bidirectional shift register, and is operating according to a control signal 916.

[0120] A latch circuit 941 latches an indicative data (getting it blocked and synchronizing with the scan selection signal 903 of a scanning circuit 902) 940 according to a control signal (latch signal) 917. This latch circuit 941 is outputting the latched data to the liquid crystal drive circuit 943 as an indicative data 942.

[0121] The liquid crystal drive circuit 943 generates the liquid crystal driver voltage 944 corresponding to an indicative data 942 by pulse width modulation. Pulse width modulation is a method which controls the electrical-potential-difference actual value given to liquid crystal by switching the electrical potential difference given to the data electrode of a liquid crystal panel 309 during a selection period, and realizes a gradation display as it is shown in drawing 16 . In the example of drawing 16 , the selection period was equally divided into three and 4 gradation displays are realized by switching the electrical potential difference given to a data electrode for every period of this equally divided into three.

[0122] An oscillator circuit 402 generates the display clock 403 for specifying display timing, and supplies it to a scanning circuit 902.

[0123] A power circuit 904 generates and supplies liquid crystal panel driver voltage (the supply voltage 405 of 902 for scanning circuits, supply voltage 906 for data driver LSI900).

[0124] In addition, the configuration and actuation of the animation controller 311 are the same as that of the 1st operation gestalt fundamentally (refer to drawing 5). however — this — unlike the 1st operation gestalt, FRC data are used as data of 2 bits of each pixel with the 2nd operation gestalt. The multi-gradation display is realized by combining the gradation control by the FRC control which the animation controller 311 performs, and the gradation control by the Pulse-Density-Modulation control which the data driver LSI 900 performs. If Pulse-Density-Modulation control performs 4 gradation control and FRC control performs control of 12 or more gradation, the display of 32 or more gradation is realizable with such combination.

[0125] Next, the display action in this operation gestalt is explained.

[0126] Explanation is divided into the display action of a still picture, and the display action of an animation, and is performed.

[0127] About a [display action of still picture] still picture, CPU304 reads and (read access) carries out the indicative data in memory 305, it is what this is written in the memory cell 933 of the data driver LSI 900 for (light access), and renewal of an indicative data (drawing) is performed. Access to memory 933 is performed at random. Access of CPU304 at this time is performed by the SRAM interface. The read/write timing of a SRAM interface is as having been shown in drawing 10 and drawing 11 .

[0128] Hereafter, the writing of the indicative data to the memory cell 933 of the data driver LSI 900 and read-out of the indicative data from a memory cell 933 are explained.

[0129] First, the writing of the indicative data to a memory cell 933 is explained.

[0130] The read/write address from a system (CPU304 grade) is inputted into the address administration circuit 908 of the data driver LSI 900 through an address bus 301. As for the address administration circuit 908 of each data driver LSI 900, based on a control signal 901, access at that time judges whether it is a thing to its data driver LSI 900 which belongs, respectively. When it is access to the data driver LSI 900 to which oneself belongs as a result of this judgment, the address 301 inputted at this time is changed into a column address 909 and a row address 910.

[0131] The column address decoder 929 decodes this column address 909. A data selector 931 chooses the data line of the corresponding address based on this decoding result.

[0132] On the other hand, a selector 923 chooses a row address 910 and outputs it to the row address decoder 925 as a row address 924. The row address decoder 925 decodes this row address 924, and chooses one gate line according to a decoding result. Thereby, CPU304 can access the predetermined bit on the memory cell 933 which becomes settled by the data line and the gate line which are then chosen, and can transmit an indicative data to the predetermined address.

[0133] Next, read-out (display action) of the indicative data from a memory cell 933 is explained.

[0134] The timing control circuit 911 is checking the contents and the row address 922 of a register 9110, and knows displaying the still picture field at this time. Therefore, the timing control circuit 911 is outputting a value as which a selector 937 chooses a data bus 934 as a control signal 945 at this time. A selector 937 chooses a data bus 934 according to this control signal 945, and outputs the data (2 bits of each pixel, and one line) read from the memory cell 933 through this data bus 934 as an indicative data 938.

[0135] A shift register 939 latches an indicative data 938 a level period. The latch circuit 941 following this is the following level period, latches the indicative data 940 which a shift register 939 outputs, and outputs it to the liquid crystal drive circuit 943 as an indicative data 942. The liquid crystal drive circuit 943 outputs the liquid crystal driver voltage 944 which performed Pulse-Density-Modulation (PWM) control according to this indicative data 942 to a liquid crystal panel 309. The output of the liquid crystal driver voltage 944 is outputted synchronizing with the scan selection signal 903 which a scanning circuit 902 generates, and, thereby, can realize the display for one line of a liquid crystal panel 309.

[0136] The display of a still picture is attained by repeating the above actuation.

[0137] In displaying a [display action of animation] animation, a multi-gradation display and the fast transfer of an indicative data are needed in practice. Since the data driver LSI 900 of this operation gestalt corresponds to this, it performs the following drawing actuation.

[0138] A video data performs animation expanding processing from animation compressed data by the animation controller 311 and CPU304, and develops it to an indicative data. As for the developed indicative data, the animation controller 311 performs FRC control.

[0139] By the way, the animation controller 311 is also equipped with the register (control register circuit 505 in drawing 5) which stored the information which shows an animation field. The animation controller 311 can know whether the animation display field is then set as the object of display processing by checking the contents of this register etc. When the animation display field is then set as the object of display processing, the animation controller 311 performs above-mentioned FRC control. And the FRC data of every one line of 2 bits of each pixel

obtained as a result are sent to the data driver LSI 900 through a data bus 302 one by one.

[0140] It gets to know that it is an animation display field that the timing control circuit 911 of the data driver LSI 900 is also then set as the object of display processing by checking the contents and the row address 922 of a register 9110 similarly. Therefore, let the timing control circuit 911 be the value as which a selector 937 chooses a data bus 302 for the control signal 945 at this time. Consequently, a selector 937 chooses the FRC data sent from the animation controller 311 through a data bus 302, and is made to output them to a shift register 939. The output of the liquid crystal driver voltage 444 to which this pulse width control was performed will be performed like the case of a still picture after this. Thus, the display of 32 or more gradation is realizable by combining 4 gradation control by pulse width modulation, and 12 gradation control by the FRC gradation method.

[0141] Next, the timing of the animation data transfer to the data driver LSI 900 and the timing of processing within the data driver LSI 900 of this video data are further explained to a detail using drawing 12 , drawing 13 , and drawing 14 from the animation controller 311.

[0142] In explanation here, the field (n<m) from n lines of a liquid crystal panel 309 to m lines shall be set up as an animation display field in the register 4110 of the timing control circuit 411 (refer to drawing 12).

[0143] The animation display data transfer from the animation controller 311 to the data driver 900 is the same as that of the 1st operation gestalt.

[0144] The animation display data of every one line of 2 bits of each pixel are transmitted to the data driver LSI 900 from the animation controller 311 through a data bus 302 at a serial. In drawing 13 , CL1 is a synchronizing signal showing a level period, and is a signal included in the display synchronizing signal 907 (refer to drawing 6 and drawing 7).

[0145] The timing control circuit 911 is outputted to the display address counter 921 by making this CL1 into a control signal 913. The display address counter 921 counts this control signal 913 (CL1), and is outputting that counted value to the selector 923 as a row address 922 for a display.

[0146] Although the selector 937 has changed the selection condition according to the control signal 945, the selection condition has the counted value and the following relation of the display address counter 921. That is, when the counted value of the display address counter 921 is n−1, the selector 937 has chosen the data bus 934 (that is, the indicative data of the n−1st line stored in the memory cell 933) (when it is not an animation display field). When the counted value of the display address counter 921 is n, the selector 937 has chosen the data bus 302 (that is, indicative data sent from the animation controller 311) (when it is an animation display field). Thus, in an animation display field, a selector 937 chooses a data bus 302 (indicative data from the animation controller 311), and the indicative data of a memory cell 933 is chosen except an animation display field.

[0147] Moreover, actuation of the animation controller 311 also has actuation and the following relation of a selector 937 and the display address counter 921. That is, when the display address counter 921 counts (n−1), the animation controller 311 carries out the sequential transfer of the indicative data of the n−th line.

[0148] In the data driver LSI 900, the data (one line) of the n−th line with which the shift register 939 has been sent from this animation controller 311 to the timing shown in drawing 14 are incorporated. That is, a shift register 939 is the shift clock 916 which synchronized with WE signal, and incorporates an indicative data 938 (the data of the n−th line sent from the animation controller 311) by one line one by one (notes: at this time, the selector 937 is made into the condition of having chosen the data bus 302 as already stated). In addition, the transfer of the indicative data from the animation controller 311 is performed synchronizing with WE signal (write enable signal) in drawing 14 . A shift register 939 transmits the data incorporated to such timing to a latch circuit 941 as an indicative data 940.

[0149] A latch circuit 941 latches this indicative data 940 synchronizing with the CL1 following signal, and transmits it to the liquid crystal drive circuit 943 as an indicative data 942 (refer to drawing 13). The liquid crystal drive circuit 943 generates and outputs the liquid crystal driver voltage 944 which performed Pulse Density Modulation corresponding to this indicative data 942 (2 bits of each pixel). The output of the liquid crystal driver voltage 944 is outputted synchronizing with the scan selection signal 903 which a scanning circuit 902 generates, and, thereby, can realize the display for one line of a liquid crystal panel 309.

[0150] A movie display becomes possible by repeating the above actuation.

[0151] as having explained above — this — in the liquid crystal display of the 2nd operation gestalt, the memory cell 933 with which the data driver LSI 900 is equipped is used only for the still picture display. Therefore, it is not necessary to rewrite a memory cell 933 at a high speed, and low-power-izing is possible. Moreover, the gradation display in a movie display is realized by combining the FRC control by the animation controller, and the Pulse-Density-Modulation control by the data driver. Therefore, animation display (this operation gestalt 32 gradation) of many gradation becomes realizable easily, without increasing the memory space of the data driver LSI 900.

[0152] Next, the liquid crystal display which is the 3rd operation gestalt is explained using drawing 8 thru/or drawing 14 , and drawing 17 .

[0153] With the 3rd operation gestalt, an electrical-potential-difference modulation technique (AM method) is used as a gradation method.

[0154] This whole liquid crystal display configuration is the same as that of the 1st operation gestalt (refer to drawing 1) except for the point using the data driver 1400 instead of the data driver 307. this — the description in the 3rd operation gestalt is mainly in the data driver LSI 1400. Then, suppose after this that it explains focusing on the data driver LSI 1400.

[0155] Each data driver LSI 1400 is equipped with the display memory (memory cell 1433) equipped with the capacity which can hold the indicative data of each pixel triplet by 240 lines only 160 ****. Therefore, a 160x240-pixel liquid crystal panel can be displayed with 8 gradation by one data driver LSI 1400. Since a liquid crystal panel 309 is 320x480 pixels, it arranges every (a total of four pieces) two of this data driver LSI 1400 up and down, and performs 2 screen drives of the upper and lower sides of every 240 lines.

[0156] The data driver LSI 1400 is equipped with the address administration circuit 1408, the timing control circuit 1411, I/O buffer 1419, the display address counter 1421, a selector 1423, the row address decoder 1425, the column address decoder 1429, a data selector 1431, a memory cell 1433, the selector 1437, the shift register 1439, the latch circuit 1441, and the liquid crystal drive circuit 1443 as shown in drawing 8 and drawing 9 . Moreover, it has the various signal lines for connecting between these each part (or between other circuit parts), buses 1420, 1432, and 1434, and 1442 grades.

[0157] In addition, the oscillator circuit 402 and power circuit 1404 which were not being omitted and drawn in drawing 1 are also drawn on this drawing 8 and drawing 9 .

[0158] The address administration circuit 1408 changes the address 301 into a column address 1409 and a row address 1410 based on control signals 303 and 1401. On the other hand, the address administration circuit 1408 is outputting the row address 1410 for the column address 1409 to the column address decoder 1429 through a selector 1423 to the row address decoder 1425. In addition, a control signal 1401 is for specifying any are the candidates for access at that time among four data drivers LSI 1400.

[0159] The timing control circuit 1411 generates the various control signals 1412, 1413, 1414, 1416, 1417, 1418, 1427, and 1445 of the data driver LSI1400 interior from a control signal 303 and the display synchronizing signal 1407. The control signal 1412 is outputted to I/O buffer 1419 among these control signals. The control signal 1413 is outputted to the display address counter 1421. The control signal 1414 is outputted to the selector 1423. The control signal (shift clock) 1416 is outputted to the shift register 1439. The control signal (latch signal) 1417 is outputted to the latch circuit 1441, and is used for controlling the timing which latches an indicative data. The control signal 1418 is outputted to the liquid crystal drive circuit 1443, and is used for controlling alternating current-ization of a liquid crystal drive. The control signal 1427 is outputted to the liquid crystal drive circuit 1443, and is used for controlling the timing of electrical-potential-difference modulation control. The control signal 1445 is outputted to the selector 1437, and is used for this selector 1437 choosing either of the two data buses (a data bus 436, data bus 302) connected to the selector 1437. In addition, the above-mentioned control signal 1401 is inputted also into the timing control circuit 1411.

[0160] This timing control circuit 1411 is equipped with the register 14110 with which the information which shows the field where an animation is displayed on a liquid crystal panel 309 was stored. Moreover, the row address 1422 which shows whether the indicative data corresponding to Rhine of what position on a liquid crystal

panel 309 should be read from a memory cell 1433 is then inputted into this timing control circuit 1411. The control signal 1445 is generated based on the contents and the row address 1422 of this register 14110. That is, in the animation display field, the control signal 1445 is generated so that an indicative data 1434 (still picture data) may be made to choose as a selector 1437 an indicative data 302 (video data sent from the animation controller 311) by the still picture viewing area on the other hand. Such a point is the focus of this operation gestalt max.

[0161] I/O buffer 1419 controls I/O of indicative datas 302 and 1420 according to a control signal 1412.

[0162] The display address counter 1421 generates the row address 1422 for a display according to a control signal 1413. This display address counter 1421 is outputting this row address 1422 to the timing control circuit 1411 and the selector 1423.

[0163] A selector 1423 chooses either the row address 1422 for a display or the row addresses 1410 for drawing according to a control signal 1414. This selector 1423 is outputting the selected one to the row address decoder 1425 as a row address 1424.

[0164] The row address decoder 1425 generates the WORD selection signal 1426 by decoding a row address 1424, and outputs this to the gate line of a memory cell 1433.

[0165] The column address decoder 1429 generates a selection signal 1430 based on the column address 1409 which the address administration circuit 1408 outputs. This column address decoder 1429 is outputting this selection signal 1430 to the data selector 1431.

[0166] A data selector 1431 is choosing the data line of the data bus 1432 of a memory cell 1433 according to a selection signal 1430, and controls I/O of the indicative data 1420 to a memory cell 1433.

[0167] A memory cell 1433 is the memory for storing temporarily an indicative data (still picture data), and consists of RAM. The field set as the object of writing/read-out of the indicative data on this memory cell 1433 can be specified now based on an above-mentioned column address and an above-mentioned row address. The memory cell 1433 is equipped with the capacity which can hold the indicative data of each pixel triplet by 240 lines only 160 **** as mentioned above.

[0168] the indicative data 302 (video data) into which the selector 1437 is inputted as the indicative data 1434 (still picture data) from the animation controller 311, and ** — inner either is chosen according to a control signal 1445. That is, in this operation gestalt, by the time the indicative data sent through a data bus 302 results in a selector 1437, the two roots will be prepared. The 1st root is after data bus 302 the root which results in a selector 1437 through I/O buffer 1419, a data selector 1431, a memory cell 1433, and a data bus 1434. The 2nd root is the root which connected the data bus 302 to the selector 1437 directly through the memory cell 1433 grade. During the period which should input the indicative data about the field beforehand set up as an animation display field, the video data is inputted into the data bus 302 from the animation controller 311. Still picture data are inputted into the data bus 302 from CPU304 and the memory 305 grade during the period which should, on the other hand, input the indicative data about the field beforehand set up as a quiescence viewing area. Therefore, in a selector 1437, either of the two roots from a data bus 302 to a selector 1437 can be chosen now according to an indicative data by choosing either a data bus 1434 or the data buses 302 according to a control signal 1445. This selector 1437 is outputted to the shift register 1439 by making into an indicative data 1438 the direction which carried out in this way and was chosen.

[0169] In addition, the concrete internal configuration of the selector 1437 in this operation gestalt is [the selector 437 in the 1st operation gestalt, and] the same (refer to drawing 4).

[0170] A shift register 1439 is a 12-bit bidirectional shift register, and is operating according to a control signal (shift clock) 1416.

[0171] A latch circuit 1441 latches an indicative data (getting it blocked and synchronizing with the scan selection signal 1403 of a scanning circuit 1402) 1440 according to a control signal (latch signal) 1417. This latch circuit 1441 is outputting the latched data to the liquid crystal drive circuit 1443 as an indicative data 1442.

[0172] The liquid crystal drive circuit 1443 generates the liquid crystal driver voltage 944 corresponding to an indicative data 1442 by the electrical-potential-difference modulation technique. An electrical-potential-

difference modulation technique is giving the halftone electrical potential difference according to gradation data to the data electrode of a liquid crystal panel 309, and is a method which controls the electrical-potential-difference actual value given to liquid crystal, and realizes a gradation display as it is shown in drawing 17 . In an electrical-potential-difference modulation technique, since the electrical potential differences given to a non-selection period differ with the gradation of an indicative data, a halftone electrical potential difference is set up so that electrical-potential-difference actual value may become fixed at two frames (refer to drawing 17). This liquid crystal drive circuit 1443 is enabling 8 gradation displays by the electrical-potential-difference modulation.

[0173] An oscillator circuit 402 generates the display clock 403 for specifying display timing, and supplies it to a scanning circuit 1402.

[0174] A power circuit 1404 generates and supplies liquid crystal panel driver voltage (the supply voltage 405 of 1402 for scanning circuits, supply voltage 1406 for data driver LSI1400).

[0175] In addition, the configuration and actuation of the animation controller 311 are the same as that of the 1st operation gestalt fundamentally (refer to drawing 5). however — this — unlike the 1st operation gestalt, FRC data are used as the data of each pixel triplet with the 3rd operation gestalt. The multi-gradation display is realized by combining the gradation control by the FRC control which the animation controller 311 performs, and the gradation control by the electrical-potential-difference modulation control which the data driver LSI 1400 performs. If electrical-potential-difference modulation control performs 8 gradation control and FRC control performs control of 6 or more gradation, the display of 32 or more gradation is realizable with such combination.

[0176] Next, the display action in this operation gestalt is explained.

[0177] Explanation is divided into the display action of a still picture, and the display action of an animation, and is performed.

[0178] About a [display action of still picture] still picture, CPU304 reads and (read access) carries out the indicative data in memory 305, it is what this is written in the memory cell 1433 of the data driver LSI 1400 for (light access), and renewal of an indicative data (drawing) is performed. Access to memory 1433 is performed at random. Access of CPU304 at this time is performed by the SRAM interface. The read/write timing of a SRAM interface is as having been shown in drawing 10 and drawing 11 .

[0179] Hereafter, the writing of the indicative data to the memory cell 1433 of the data driver LSI 1400 and read-out of the indicative data from a memory cell 1433 are explained.

[0180] First, the writing of the indicative data to a memory cell 1433 is explained.

[0181] The read/write address from a system (CPU304 grade) is inputted into the address administration circuit 1408 of the data driver LSI 1400 through an address bus 301. As for the address administration circuit 1408 of each data driver LSI 1400, based on a control signal 1401, access at that time judges whether it is a thing to its data driver LSI 1400 which belongs, respectively. When it is access to the data driver LSI 1400 to which oneself belongs as a result of this judgment, the address 301 inputted at this time is changed into a column address 1409 and a row address 1410.

[0182] The column address decoder 1429 decodes this column address 1409. A data selector 1431 chooses the data line of the corresponding address based on this decoding result.

[0183] On the other hand, a selector 1423 chooses a row address 1410 and outputs it to the row address decoder 1425 as a row address 1424. The row address decoder 1425 decodes this row address 1424, and chooses one gate line according to a decoding result. Thereby, CPU304 can access the predetermined bit on the memory cell 1433 which becomes settled by the data line and the gate line which are then chosen, and can transmit an indicative data to the predetermined address.

[0184] Next, read-out (display action) of the indicative data from a memory cell 1433 is explained.

[0185] The timing control circuit 1411 is checking the contents and the row address 1422 of a register 14110, and knows displaying the still picture field at this time. Therefore, the timing control circuit 1411 is outputting a value as which a selector 1437 chooses a data bus 1434 as a control signal 1445 at this time. A selector 1437 chooses a data bus 1434 according to this control signal 1445, and outputs the data (each pixel triplet and one line) read from the memory cell 1433 through this data bus 1434 as an indicative data 1438.

[0186] A shift register 1439 latches an indicative data 1438 a level period. The latch circuit 1441 following this is the following level period, latches the indicative data 1440 which a shift register 1439 outputs, and outputs it to the liquid crystal drive circuit 1443 as an indicative data 1442. The liquid crystal drive circuit 1443 outputs the liquid crystal driver voltage 1444 which performed electrical-potential-difference modulation (AM) control according to this indicative data 1442 to a liquid crystal panel 309. The output of the liquid crystal driver voltage 1444 is outputted synchronizing with the scan selection signal 1403 which a scanning circuit 1402 generates, and, thereby, can realize the display for one line of a liquid crystal panel 309.
[0187] The display of a still picture is attained by repeating the above actuation.
[0188] In displaying a [display action of animation] animation, a multi-gradation display and the fast transfer of an indicative data are needed in practice. Since the data driver LSI 1400 of this operation gestalt corresponds to this, it performs the following drawing actuation.
[0189] A video data performs animation expanding processing from animation compressed data by the animation controller 311 and CPU304, and develops it to an indicative data. As for the developed indicative data, the animation controller 311 performs FRC control.
[0190] By the way, the animation controller 311 is also equipped with the register (control register circuit 505 in drawing 5) which stored the information which shows an animation field. The animation controller 311 can know whether the animation display field is then set as the object of display processing by checking the contents of this register etc. When the animation display field is then set as the object of display processing, the animation controller 311 performs above-mentioned FRC control. And the FRC data of every one line of each pixel triplet obtained as a result are serially sent to the data driver LSI 1400 through a data bus 302 one by one.
[0191] It gets to know that it is an animation display field that the timing control circuit 1411 of the data driver LSI 1400 is also then set as the object of display processing by checking the contents and the row address 1422 of a register 14110 similarly. Therefore, let the timing control circuit 1411 be the value as which a selector 1437 chooses a data bus 302 for the control signal 1445 at this time. Consequently, a selector 1437 chooses the FRC data sent from the animation controller 311 through a data bus 302, and is made to output them to a shift register 1439. The output of the liquid crystal driver voltage 444 to which this electrical-potential-difference modulation control was performed will be performed like the case of a still picture after this. Thus, the display of 32 or more gradation is realizable by combining 8 gradation control by the electrical-potential-difference modulation technique, and the control of 6 or more gradation by the FRC gradation method.
[0192] Next, the timing of the animation data transfer to the data driver LSI 1400 and the timing of processing within the data driver LSI 1400 of this video data are further explained to a detail using drawing 12 , drawing 13 , and drawing 14 from the animation controller 311.
[0193] In explanation here, the field (n<m) from n lines of a liquid crystal panel 309 to m lines shall be set up as an animation display field in the register 4110 of the timing control circuit 411 (refer to drawing 12).
[0194] The animation display data transfer from the animation controller 311 to the data driver 1400 is the same as that of the 1st operation gestalt.
[0195] The animation display data of every one line of each pixel triplet are transmitted to the data driver LSI 1400 from the animation controller 311 through a data bus 302 at a serial. In drawing 13 , CL1 is a synchronizing signal showing a level period, and is a signal included in the display synchronizing signal 1407 (refer to drawing 8 and drawing 9).
[0196] The timing control circuit 1411 is outputted to the display address counter 1421 by making this CL1 into a control signal 1413. The display address counter 1421 counts this control signal 1413 (CL1), and is outputting that counted value to the selector 1423 as a row address 1422 for a display.
[0197] Although the selector 1437 has changed the selection condition according to the control signal 1445, the selection condition has the counted value and the following relation of the display address counter 1421. That is, when the counted value of the display address counter 1421 is n-1, the selector 1437 has chosen the data bus 1434 (that is, the indicative data of the n-1st line stored in the memory cell 1433) (when it is not an animation display field). When the counted value of the display address counter 1421 is n, the selector 1437 has chosen the

data bus 302 (that is, indicative data sent from the animation controller 311) (when it is an animation display field). Thus, in an animation display field, a selector 1437 chooses a data bus 302 (indicative data from the animation controller 311), and the indicative data of a memory cell 1433 is chosen except an animation display field.

[0198] Moreover, actuation of the animation controller 311 also has actuation and the following relation of a selector 1437 and the display address counter 1421. That is, when the display address counter 1421 counts (n−1), the animation controller 311 carries out the sequential transfer of the indicative data of the n−th line.

[0199] In the data driver LSI 1400, the data (one line) of the n−th line with which the shift register 1439 has been sent from this animation controller 311 to the timing shown in drawing 14 are incorporated. That is, a shift register 1439 is the shift clock 1416 which synchronized with WE signal, and incorporates an indicative data 1438 (the data of the n−th line sent from the animation controller 311) by one line one by one (notes: at this time, the selector 1437 is made into the condition of having chosen the data bus 302 as already stated). In addition, the transfer of the indicative data from the animation controller 311 is performed synchronizing with WE signal (write enable signal) in drawing 14 . A shift register 1439 transmits the data incorporated to such timing to a latch circuit 1441 as an indicative data 1440.

[0200] A latch circuit 1441 latches this indicative data 1440 synchronizing with the CL1 following signal, and transmits it to the liquid crystal drive circuit 1443 as an indicative data 1442 (refer to drawing 13). The liquid crystal drive circuit 1443 generates and outputs the liquid crystal driver voltage 1444 which performed the electrical−potential−difference modulation corresponding to this indicative data 1442 (each pixel triplet). The output of the liquid crystal driver voltage 1444 is outputted synchronizing with the scan selection signal 1403 which a scanning circuit 1402 generates, and, thereby, can realize the display for one line of a liquid crystal panel 309.

[0201] A movie display becomes possible by repeating the above actuation.

[0202] as having explained above — this — in the liquid crystal display of the 3rd operation gestalt, the memory cell 1433 with which the data driver LSI 1400 is equipped is used only for the still picture display. Therefore, it is not necessary to rewrite a memory cell 1433 at a high speed, and low−power−izing is possible. Moreover, the gradation display in a movie display is realized by combining the FRC control by the animation controller, and the electrical−potential−difference modulation control by the data driver. Therefore, animation display (this operation gestalt 32 gradation) of many gradation becomes realizable easily, without increasing the memory space of the data driver LSI 1400.

[0203] the 1− described above — with the 3rd operation gestalt, although the number of outputs of a data driver was set to 160, the number of outputs is not limited to this. It can respond easily only by changing the configuration of memory, an output circuit, etc. corresponding to the number of outputs. Moreover, other combination of gradation control of FRC, Pulse Density Modulation, and an electrical−potential−difference modulation can respond easily.

[0204] The configuration of the 1st, 2nd, and 3rd operation gestalt mentioned above may be combined, respectively. For example, it may be made to perform gradation control by a total of three places of location [just behind a memory cell], animation controller, and liquid crystal drive circuit **.

[0205] If the data driver and liquid crystal display which were described above are used, power consumption will be small and the possible information processor of a multi−gradation display and a movie display will be obtained.

[0206] With the "data bus" said in a claim, it is equivalent to a data bus 302 in an above−mentioned operation gestalt. With an "address bus", it is equivalent to an address bus 301. It is equivalent to the address administration circuit 408 (908 1408), the column address decoder 429 (929 1429), a selector 431 (931 1431), I/O buffer 419 (919 1419), a memory cell 433 (933 1433), the row address decoder 425 (925 1425), a selector 423 (923 1423), a data bus 436 (934 1434), etc. at a "data−processing system." With "display memory", it is equivalent to a memory cell 433 (933 1433). With an "output bus", it is equivalent to a data bus 436 (934 1434). With "the 1st gradation control circuit", it is equivalent to the FRC data circuit 427 and the FRC selector 435. With a "selection means", it is equivalent to the timing control circuit 411 (911 1411), a selector 437 (937 1437), the display address counter 421 (921 1421), etc. "memory" — a register 4110 (9110 14110) — moreover,

"selection information" is equivalent to the setting information which shows the animation field stored in these registers 4110 (9110 14110). With a "directions circuit", it is equivalent to a timing control circuit (911 1411) and the display address counter 421 (921 1421). With "selection directions", it is equivalent to a control signal 445 (945 1445). It is ["selector"] equivalent to a shift register 439 (939 1439), a latch circuit 441 (941 1441), and the liquid crystal drive circuit 443 (943 1443) with a selector 437 (937 1437) "a voltage-output means." With "the 2nd gradation control circuit", it is equivalent to the part about the gradation control included in the liquid crystal drive circuit 943 (1443). With a "data controller", it is equivalent to the animation controller 311. With "the 3rd control circuit", it is equivalent to the FRC control circuit 506.

[0207] However, the definition which each part of the above cooperates closely mutually, operates, and was described here is not strict.

[0208]

[Effect of the Invention] According to this invention, a multi-gradation display and a movie display are possible, without making the display memory capacity built in a data driver increase as explained above. Moreover, since display memory is built in the data driver, the access frequency of display memory can be low-speed-ized about a still picture (it is 1 time to a level period). Therefore, low cost and low-power-ization can be reconciled. Since the number of gradation displays carries out FRC control by the external controller, it can be set as arbitration regardless of the data driver LSI. If the data driver of this invention and a liquid crystal display are used, power consumption will be small and the possible information processor of a multi-gradation display and a movie display will be obtained.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the whole liquid crystal display configuration which is the 1st operation gestalt of this invention.

[Drawing 2] It is the block diagram showing the detailed configuration of the principal part of a liquid crystal display.

[Drawing 3] It is the block diagram showing the detailed configuration of the data driver LSI 307.

[Drawing 4] It is the circuit diagram showing the internal configuration of a selector 437.

[Drawing 5] It is the block diagram showing the internal configuration of the animation controller 311.

[Drawing 6] It is drawing showing the configuration of the principal part of the liquid crystal display in the 2nd operation gestalt of this invention.

[Drawing 7] It is drawing showing the configuration of the data driver LSI 900.

[Drawing 8] It is drawing showing the configuration of the principal part of the liquid crystal display in the 3rd operation gestalt of this invention.

[Drawing 9] It is drawing showing the internal configuration of the data driver LSI 1400.

[Drawing 10] It is drawing showing the memory light timing of a SRAM interface.

[Drawing 11] It is drawing showing the memory lead timing of a SRAM interface.

[Drawing 12] It is drawing showing the thing animation display field in a liquid crystal panel 309.
[Drawing 13] It is drawing showing the animation display data transfer timing from the animation controller 311 to the liquid crystal driver 307 (900 1400).
[Drawing 14] It is drawing showing the transfer timing of the indicative data based on a shift register 439 (939 1439).
[Drawing 15] It is drawing showing an FRC gradation method.
[Drawing 16] It is drawing showing a Pulse-Density-Modulation gradation method.
[Drawing 17] It is drawing showing an electrical-potential-difference modulation gradation method.
[Drawing 18] It is the block diagram of the conventional liquid crystal display.
[Drawing 19] It is the block diagram of the principal part of the liquid crystal display of the conventional technique.
[Drawing 20] It is the block diagram of the data driver of the conventional technique.
[Description of Notations]
[Drawing 1] 301 [— CPU, 305 / — Memory, 306 / — An I/O device, 307 / — A data driver, 308 / — A scanning circuit, 309 / — A liquid crystal panel, 310 / — A display synchronizing signal, 311 / — Animation controller] — An address bus, 302 — A data bus (indicative data), 303 — A control signal, 304
[Drawing 2 and drawing 3] 401 — A control signal, 402 — An oscillator circuit, 403 — Display clock, 404 [— Scan selection signal,] — A power circuit, 405 — Supply voltage, 406 — Supply voltage, 407 408 — A address administration circuit, 409 — A column address, 410 — Row address, 411 — A timing control circuit, 412 — A control signal, 413 — Control signal, 414 [— Control signal (latch signal),] — A control signal, 415 — A control signal, 416 — A shift clock, 417 418 — A control signal, 419 — An I/O buffer, 420 — Data bus, 421 — A display address counter, 422 — A row address, 423 — Selector, 424 — A row address, 425 — A row address decoder, 426 — Selection signal, 427 — An FRC data circuit, 428 — FRC data, 429 — Column address decoder, 430 — A selection signal, 431 — A data selector, 432 — Data bus, 433 — A memory cell, 434 — A data bus (indicative data), 435 — FRC selector, 436 — A data bus (indicative data), 437 — A selector, 438 — Data bus (indicative data), 439 [— A data bus (indicative data), 443 / — A liquid crystal drive circuit, 444 / — Liquid crystal driver voltage, 445 / — A control signal, 4110 / — Register] — A shift register, 440 — A data bus (indicative data), 441 — A latch circuit, 442
[drawing 5] a 501 — timing control circuit, a 502 — I/O-hardware-control circuit, and 503 — an address control circuit, a 504 — animation processing circuit, a 505 — control register circuit, and 506 — an FRC control circuit, a 507 — control signal, a 508 — control signal, and 509 — a control signal, a 510 — control signal, a 511 — control signal, and 512 — a control signal (register latch signal), a 513 — address bus, a 514 — address bus, and 515 — — a data bus, a 516 — data bus, a 517 — data bus, and 518 — — a data bus, a 519 — data bus, and a 520 — data bus
[Drawing 6 and drawing 7] 900 — A data driver, 901 — A control signal, 902 — Scanning circuit, 903 [— Supply voltage,] — A scan selection signal, 904 — A power circuit, 1405 — Supply voltage, 1406 907 — A display synchronizing signal, 908 — A address administration circuit, 909 — Column address, 910 — A row address, 911 — A timing control circuit, 912 — Control signal, 913 — A control signal, 914 — A control signal, 916 — Control signal (shift clock), 917 — A control signal (latch signal), 918 — A control signal, 919 — I/O buffer, 920 — A data bus, 921 — A display address counter, 922 — Row address, 923 — A selector, 924 — A row address, 925 — Row address decoder, 926 — A WORD selection signal, 927 — A control signal, 929 — Column address decoder, 930 [— Memory cell,] — A selection signal, 931 — A selector, 932 — A data bus, 933 934 [— Shift register,] — A data bus, 937 — A selector, 938 — A data bus, 939 940 [— A liquid crystal drive circuit, 944 / — Liquid crystal driver voltage, 945 / — A control signal, 9110 / — Register] — A data bus (indicative data), 941 — A latch circuit, 942 — A data bus (indicative data), 943
[Drawing 8 and drawing 9] 1400 — A data driver, 1401 — A control signal, 1402 — Oscillator circuit, 1403 — A scan selection signal, 1404 — A power circuit, 1405 — Supply voltage, 1406 — Supply voltage, 1407 — A display synchronizing signal, 1408 — Address administration circuit, 1409 — A column address, 1410 — A row address, 1411 — Timing control circuit, 1412 [— Control signal (shift clock),] — A control signal, 1413 — A control

signal, 1414 — A control signal, 1416 1417 — A control signal (latch signal), 1418 — A control signal, 1419 — I/O buffer, 1420 — A data bus, 1421 — A display address counter, 1422 — Row address, 1423 — A selector, 1424 -– A row address, 1425 — Row address decoder, 1426 — A WORD selection signal, 1427 — A control signal, 1429 — Column address decoder, 1430 — A selection signal, 1431 — A data selector, 1432 — Data bus, 1433 — A memory cell, 1434 — A data bus, 1437 — Selector, 1438 [— A latch circuit, 1442 / — A data bus, 1443 / — A liquid crystal drive circuit, 1444 / — Liquid crystal driver voltage, 1445 / — A control signal, 14110 / — Register] — A data bus (indicative data), 1439 — A shift register, 1440 — A data bus, 1441

[Drawing 18] 101 [— CPU, 105 / — Memory, 106 / — An I/O device, 107 / — A data driver, 108 / — A scanning circuit, 109 / — A liquid crystal panel, 110 / — Display synchronizing signal] — An address bus, 102 — A data bus, 103 — A control signal line (control signal), 104

[Drawing 19 and drawing 20] 201 — The oscillator circuit for a display, 202 — A power circuit, 203 — Control signal line, 204 [— Address administration circuit,] — A display-control signal line, 205 — Supply voltage, 206 -– Supply voltage, 207 208 — A column address, 209 — A row address, 210 — Timing control circuit, 211 [— Control signal (latch signal),] — A control signal, 212 — A control signal, 213 — A control signal, 214 215 — A control signal (latch signal), 216 — A control signal, 217 — Display address counter, 218 — A row address, 219 -– An I/O buffer, 220 — Data bus, 221 — A selector, 222 — A row address, 223 — Column address decoder, 224 — A selection signal, 225 — A data selector, 226 — Data bus, 227 — A row address decoder, 228 — A WORD selection signal, 229 — Memory cell, 230 — A data bus (indicative data), 231 — A control signal, 232 — FRC data circuit, 233 [— A latch circuit, 237 / — A data bus, 238 / — A latch circuit, 239 / — A data bus, 240 / — A liquid crystal drive circuit, 241 / — Liquid crystal driver voltage] — FRC data, 234 — An FRC selector, 235 — A display data bus, 236

[Translation done.]